DESIGN OF THE STREAMING PROCESSOR ARCHITECTURE FOR MICROKERNEL CONTROLLER AND ALU

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Specially dedicated to my wife, Emmy, my little boy, Umar, and my mother, Azizah.

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ABSTRACT

Media application such as 3D graphic processing, image processing, video decode and encode requires high rates of arithmetic operation per second. As an outcome of a decade long research, Stream Processor architecture, which is designed to exploit the characteristic of media processing was proposed. A few architectures of stream processor had been proposed and among the popular streaming processor architecture was Imagine Stream Processor. This project is focusing on implementing Imagine-based stream processor architecture on Altera Cyclone IV GX FPGA specifically for ALU Clusters and Microkernel Controller modules. This project report presents the literature reviews of books, theses and papers regarding stream processor architecture and its related use cases. This report also documents the complete project methodology taken in order to design a stream processor on the FPGA where the design of the Stream Processor is using RTL design methodology and System Verilog Language. This report also detailed the architectural design of the stream processor in Chapter 3. Furthermore, result and discussion of the experimental work involve in this project also reported in Chapter 4. The project report concluded that an FPGA-based stream processor is successfully designed and tested with specific image processing use cases. This project report also described possible enhancements possible on the stream processor design.

ABSTRAK

Aplikasi media seperti pemprosesan grafik tiga dimensi, pemprosesan imej, penyahkodan dan pengkodan video memerlukan kadar operasi aritmetik persaat yang tinggi. Hasil daripada penyelidikan lebih satu dekad, Pemproses Aliran yang direka untuk mengekploitasi ciri-ciri pemprosesan media, telah dicadangkan. Antara beberapa reka bentuk Pemproses Aliran sudah dicadangkan, reka bentuk yang agak dikenali adalah Pemproses Aliran Imagine. Projek ini lebih fokus kepada mencipta Pemproses Aliran berasaskan seni reka Imagine di dalam Altera Cyclone IV GX FPGA terutamanya modul Kluster ALU dan Pengawal Mikrokernel. Laporan projek ini mempersembahkan kajian penulisan tentang buku-buku, tesis-tesis, dan kertas kerja berkenaan seni reka Pemproses Aliran dan pengunaannya. Laporan ini juga melaporkan methodologi penuh yang digunakan untuk mereka satu reka bentuk Pemproses Aliran di dalam satu FPGA, dimana rekaan RTL dan Bahasa System Verilog telah digunakan. Laporan ini juga menjelaskan reka bentuk Pemproses Aliran di dalam Bab ke-3. Juga, hasil dan perbincangan tentang kerja eksperimen yang terlibat dalam project ini dilaporkan dalam Bab ke-4. Laporan project ini membuat kesimpulan bahawa sebuah Pemprosesan Aliran berasaskan FPGA adalah berjaya direka and diuji dengan kes-kes ujian pemprosesan imej yang spesifik. Laporan projek ini juga menerangkan pembaikan yang boleh dilakukan keatas Pemproses Aliran tersebut.